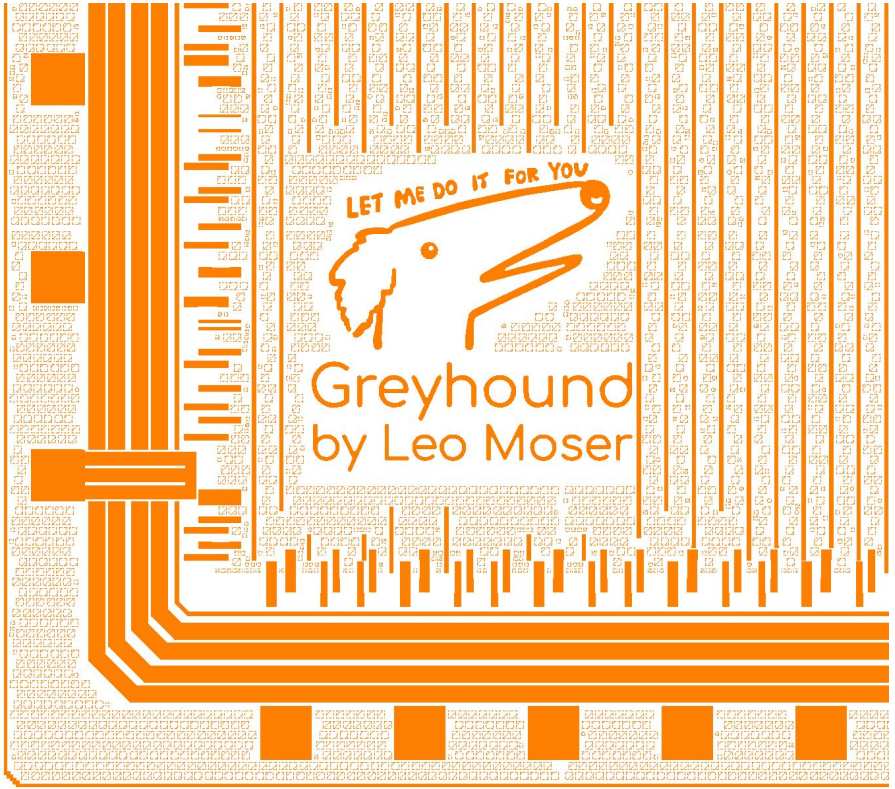
Greyhound

A RISC-V SoC with tightly coupled eFPGA on IHP SG13G2



About Me - Leo Moser

- Open Source Silicon Advocate!
- Submitted to several Open MPW shuttles
- Master's at Graz University of Technology
  - Greyhound as master's thesis
- Work @ Efabless
  - CACE - Circuit Automatic Characterization Engine
  - magic & netgen bringup for the IHP Open PDK
  - IHP OpenLane 2 support → LibreLane!
- Leo @ FOSSi Chat: https://fossi-chat.org

@leo:fossi-chat.org

Open Source Silicon - The Story So Far

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- June 2020: sky130 PDK released

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- June 2020: sky130 PDK released
- Dec 2022: gf180mcu PDK released
- Since 2023: ihp-sg13g2 PDK released
  - IHP SG13G2 BiCMOS
  - In active development

Open Source Tapeout Programs

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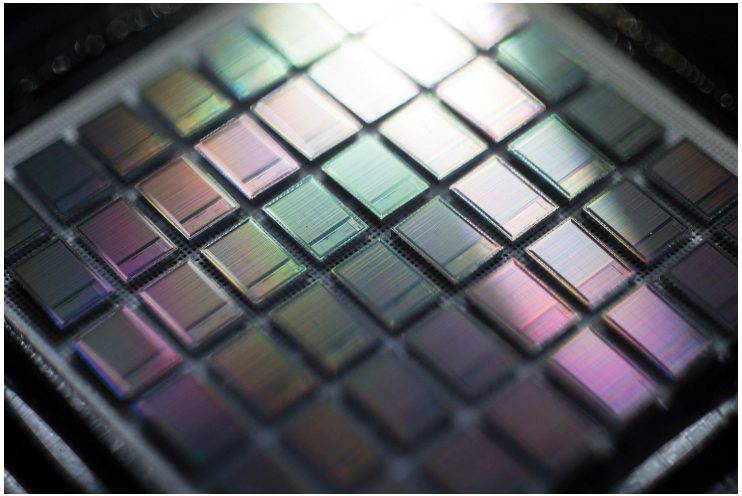
- Open MPW tapeout program
  - Google-sponsored, Efabless-managed
  - MPW-1 to MPW-8, GFMPW-0 to GFMPW-1
  - Initial issues, but chips worked!



Bare dies from MPW-6

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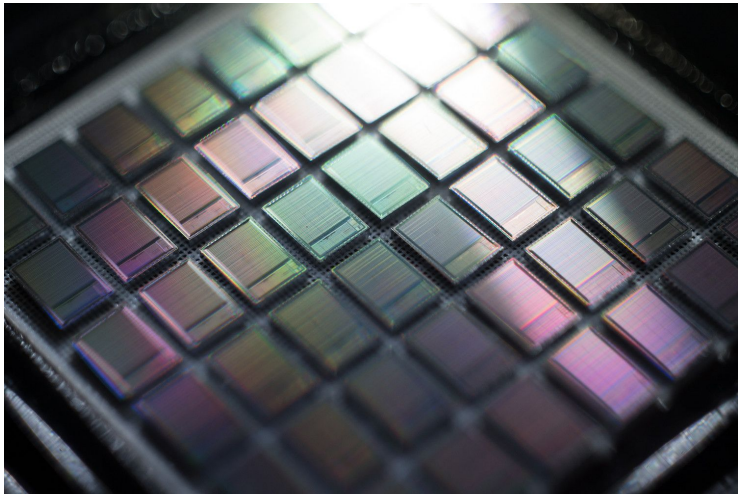

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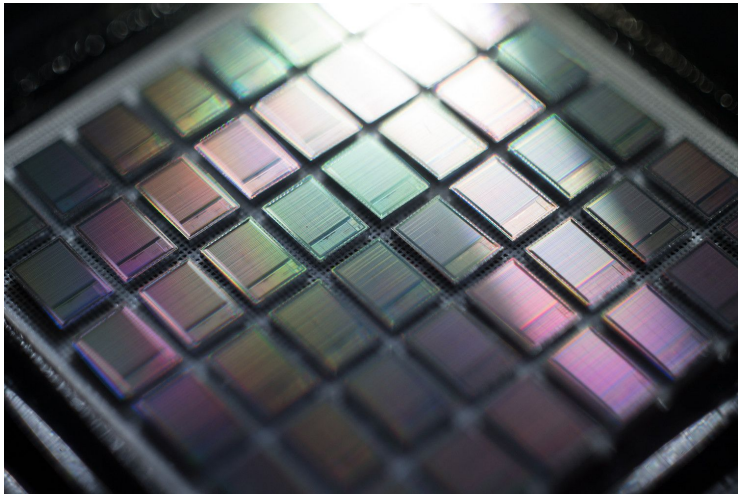
- Tiny Tapeout
  - A shared silicon tapeout platform
  - Hundreds of projects on a single die



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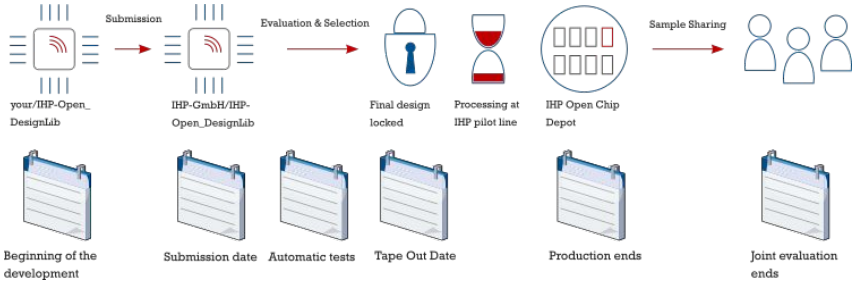

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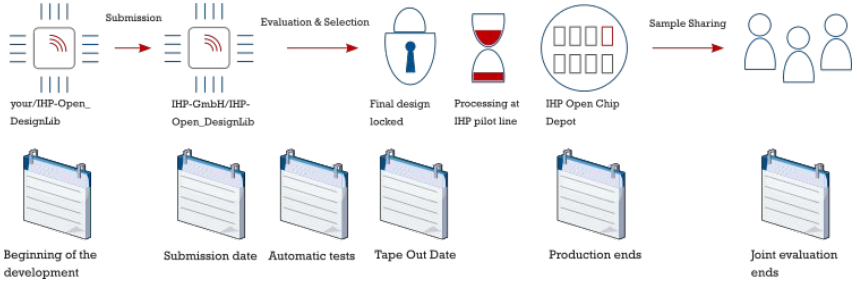

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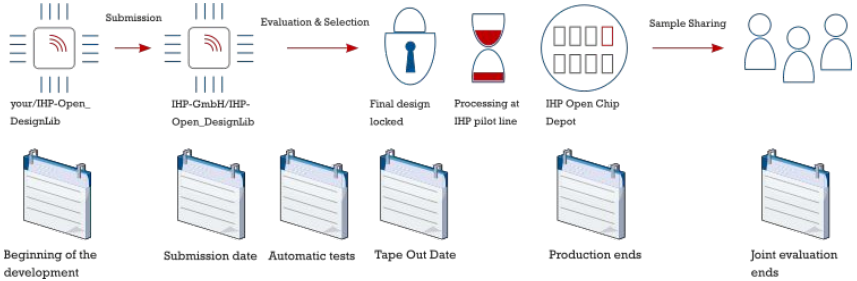
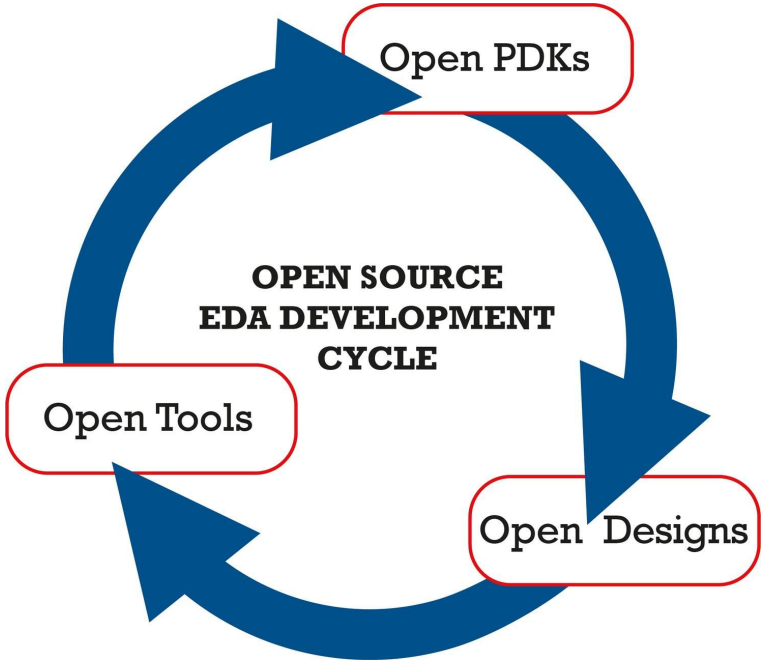
- wafer.space
  - GF180MCU
  - To be announced



- Revolution in education
- Students can freely access EDA tools, PDKs, and designs
- Chip design becomes attractive again!

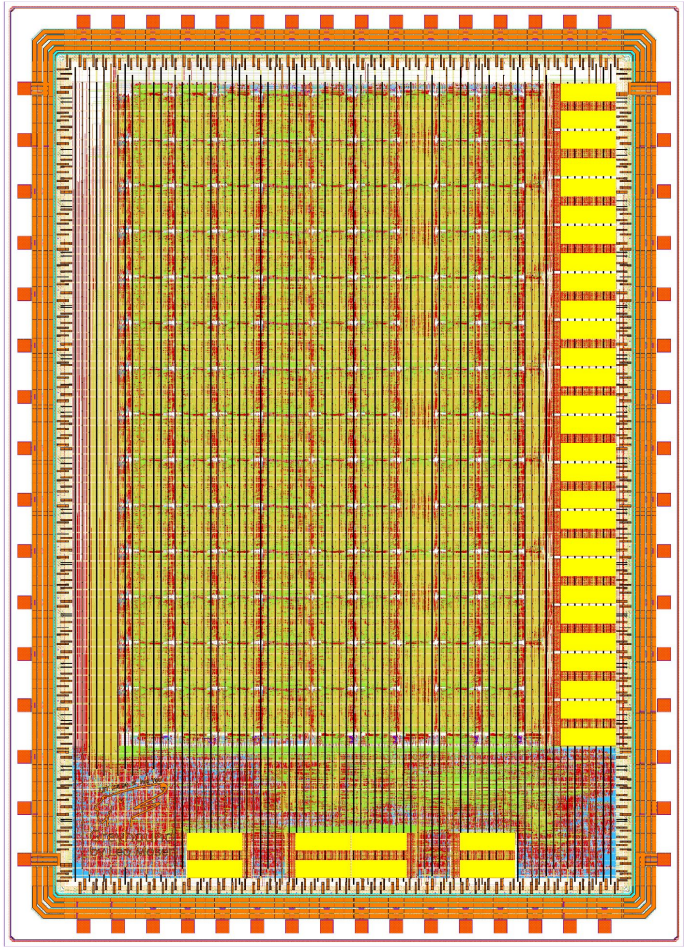


R. Scholz et al., “Update on IHP open source PDK initiative” FSiC2024

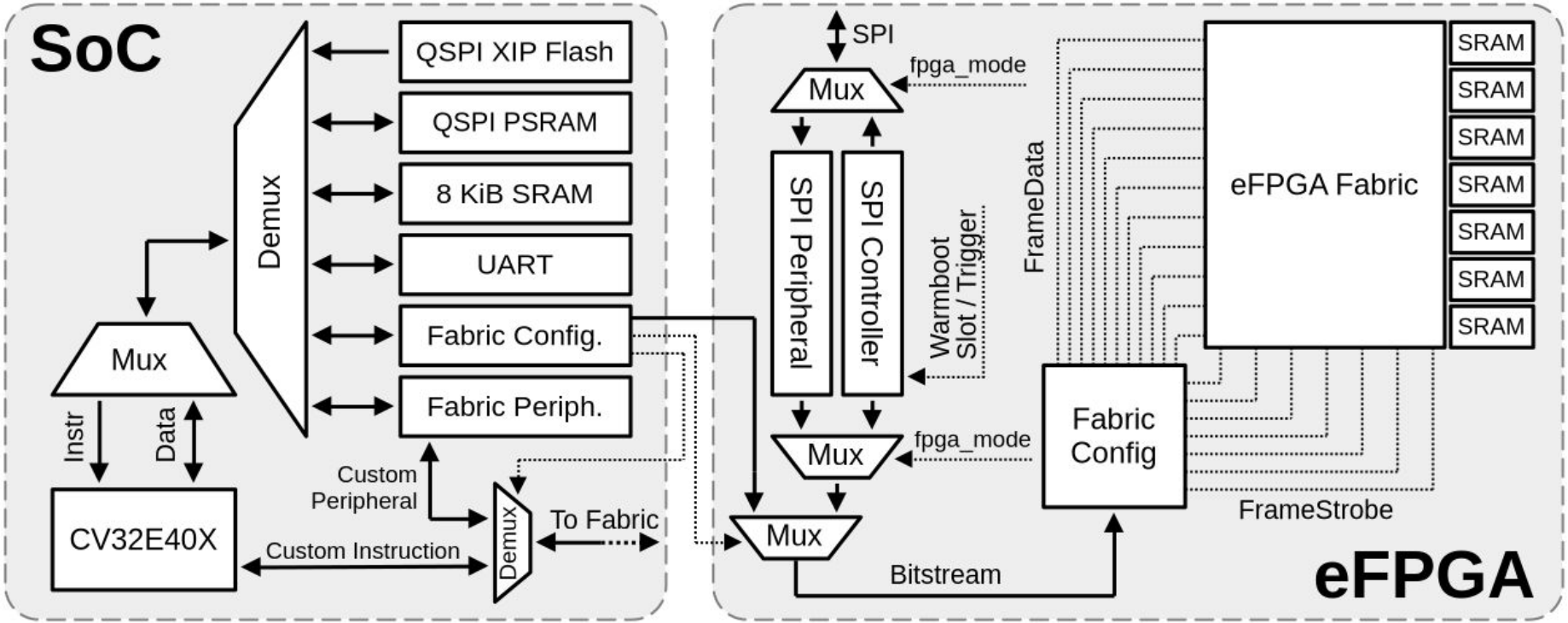
Introducing Greyhound

The Key Points

- RISC-V SoC: CV32E40X
- eFPGA fabric: FABulous
  - Custom instruction extension
  - Custom peripheral
  - Standalone FPGA
- Implemented with LibreLane!
- IHP Open PDK: SG13G2 130nm BiCMOS
- Open Source:
  - https://github.com/mole99/greyhound-ihp
- Manufactured at IHP’s pilot line

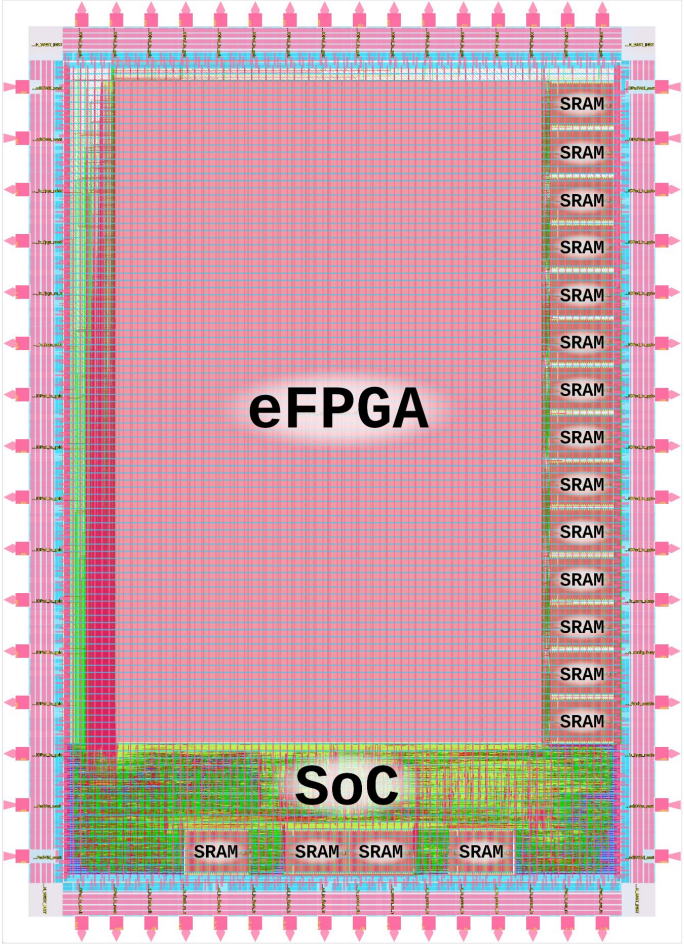


Top-Level Block Diagram



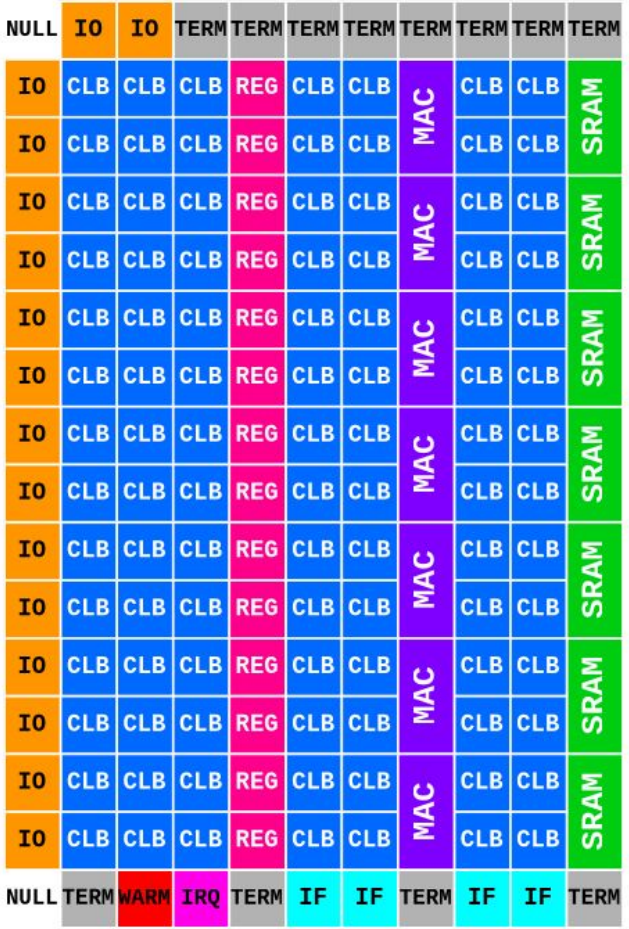
System on Chip

- RISC-V core: CV32E40X
  - RV32IMAC
  - Zca_Zcb_Zcmp_Zcmt (code-size reduction)
  - Zba_Zbb_Zbc_Zbs (bit manipulation)
  - Zicntr, Zicsr, Zihpm, Zifencei
- 8 KiB of built-in SRAM
- QSPI XIP Flash controller
  - Cache: 8 lines of 32 bytes, direct-mapped
- QSPI PSRAM controller
- Highly configurable UART
- Configure and access the eFPGA



FABulous eFPGA Fabric

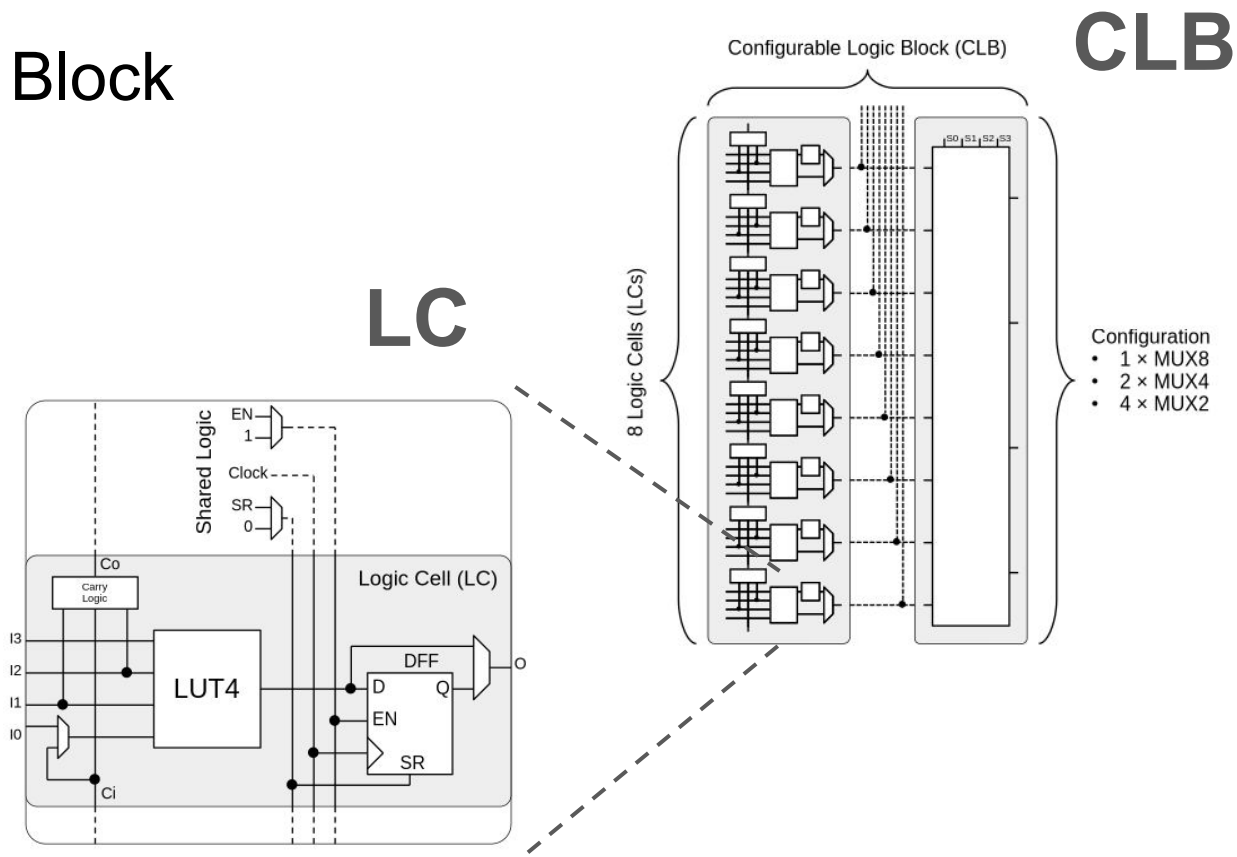
- FABulous tiles
  - 32 I/Os
  - 784 LUT4 + FF (w. carry chain)
  - 98 MUX (1×MUX8, 2×MUX4 or 4×MUX2)
  - 7 SRAM (1024×32, bit-enable, single-ported)
  - 7 MAC (8bit · 8bit + 20bit)
  - 14 Register file (32×4, 1w2r)
  - 1 Global clock network
- Custom tiles
  - 1 WARMBOOT (16 slots)
  - 1 CPU_IRQ (4×IRQs)
  - 4 CPU_IF (CPU/SoC)



Configurable Logic Block

- One CLB consists of
  - 8 Logic Cells
  - 1 Multiplexer

- One LC consists of
  - Carry chain
  - LUT4
  - D-FF
  - Shared Logic

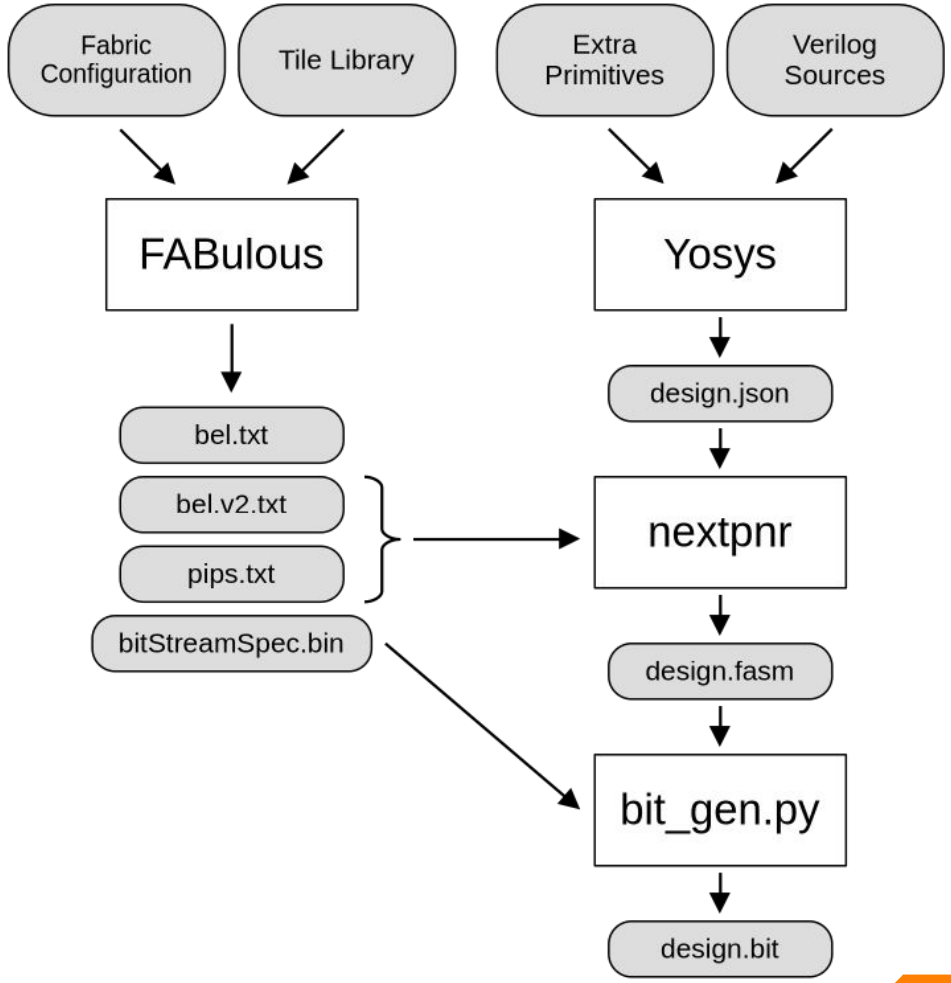


User Designs

- Yosys & nextpnr toolchain
- + fasm python package
- RISC-V designs
  - QERV (4-bit variant)
  - FazyRV (1-bit variant)

	LC usage	
FPGA	**QERV**	**FazyRV**
Greyhound	720 (92%)	754 (96%)
iCE40 UP5K	709	634

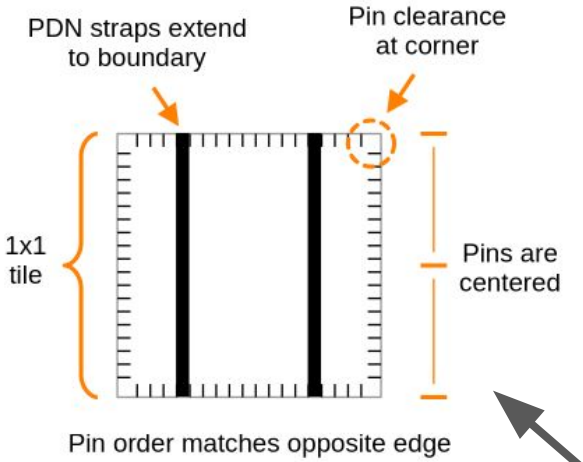
LC usage comparison



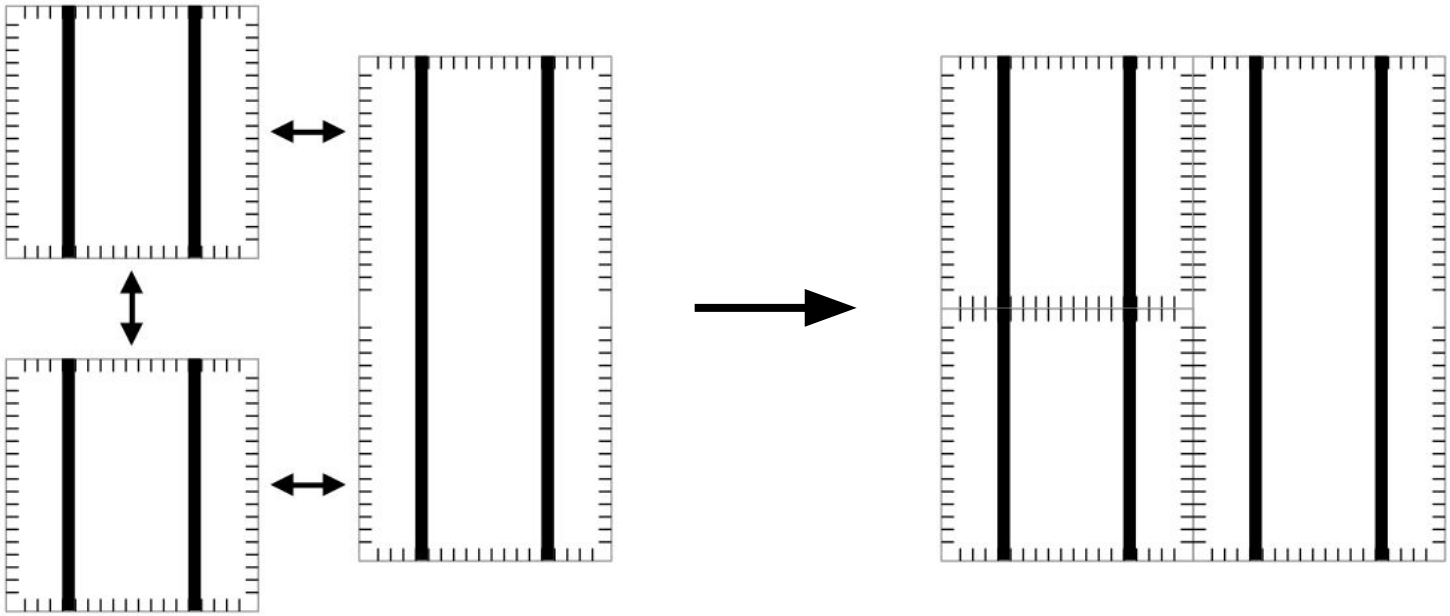
Physical Implementation

FABulous Plugin

- Integrates into LibreLane
- Custom steps / flows
  - FABulousTile
  - FABulousFabric
- Custom configuration variables
  - FABULOUS_TILE_LIBRARY
  - FABULOUS_FABRIC_CONFIG
  - FABULOUS_TILE_SIZES

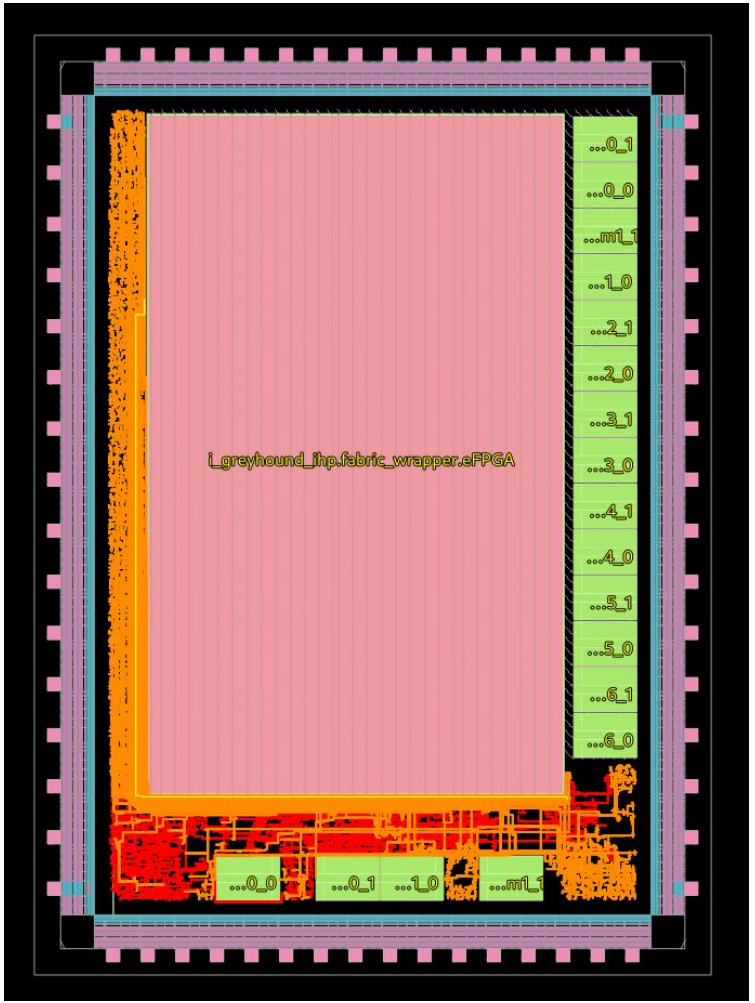


Stitching the Fabric



Implementing the Chip

- Proved to be difficult!
- Hold violations everywhere?
  - RC-estimate vs. SPEF extraction
  - Clock tree was skewed
- Workaround: Limit core area
- Solution:
  - Bugfix in OpenROAD
  - Vertical layer resistance in clock net was not considered
  - Thanks Donn!



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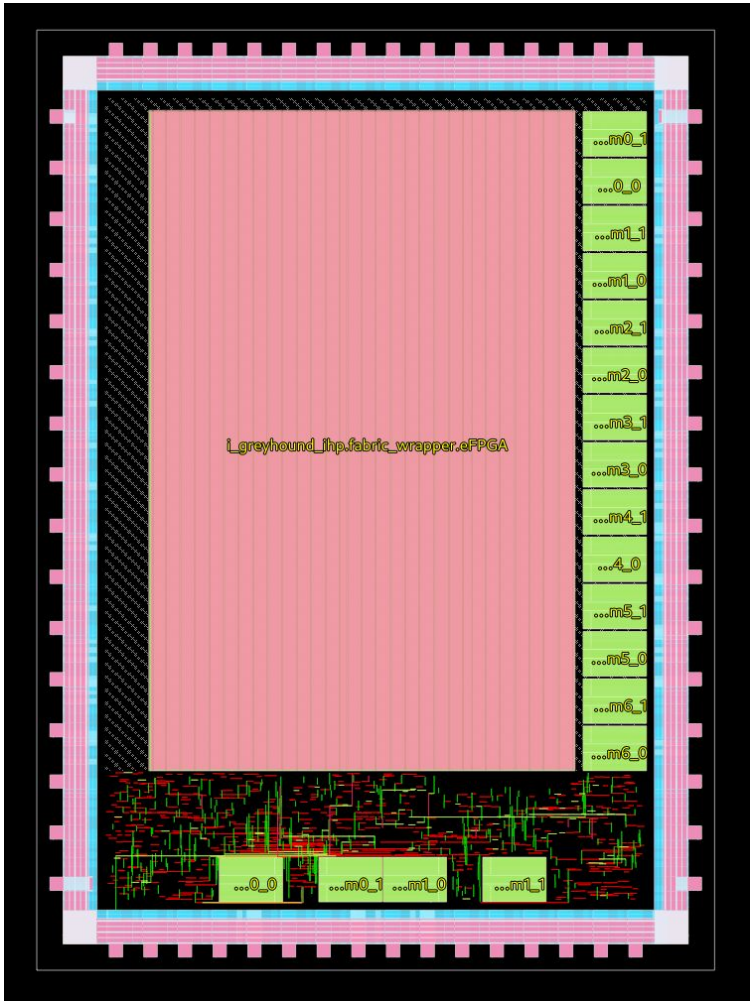

Verification

Verification - Will it work?

- Testbenches with cocotb!
- Simulations:
  - SoC on its own: RTL & GL ✅
  - Fabric on its own: RTL ✅
  - Chip top-level: RTL & GL* ✅
- Abstract LVS ✅
- Minimal DRC ✅

*only SoC, fabric is always RTL

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corner	frequency
nom_fast_1p32V_m40C	85 MHz
nom_typ_1p20V_25C	55 MHz
nom_slow_1p08V_125C	34 MHz

STA results for the SoC

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Fingers crossed 🤞

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Acknowledgements

- Graz University of Technology
  - Tobias Scheipel
  - Meinhard Kissich
- FABulous Team
  - Heidelberg University
  - University of Manchester
- Open Source Team @ IHP
- Tim Edwards @ Open Circuit Design
- BMFTR: FMD-QNC (16ME083)

The Future of Greyhound

- Next revision
  - Update to LibreLane
    - Newer OpenROAD
    - Better antenna / jumper insertion
  - Use the new standard cells
- Future revision?
  - BRAM instead of SRAM
  - Better custom instructions
  - More clock domains
  - Timing annotation
- Excited about the future!

Questions?

https://github.com/mole99/greyhound-ihp